

ABSTRACT OF THE DISCLOSURE

An input stage includes switched capacitors for analog-digital converters. The stage comprises a first switched capacitor circuit structure suitable for sampling an analog signal in input to the converter with a preset sampling period, a buffer having in input the analog signal and that can be connected to the first circuit structure by means of a first and a second sampling switch of the first circuit structure coupled respectively with the output terminal and the input terminal of the buffer. The first and the second switch are controlled respectively by a first and a second signal to close respectively for a first interval of time and for a successive second interval of time of a first semi-sampling period of the analog signal. The stage comprises a second switched capacitor circuit structure connected to a reference voltage and to the buffer and suitable for generating the second signal with a value of voltage greater in absolute value than the value of the analog signal for the duration of the second interval of time of the semi-sampling period.

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